CLAIMS

1. (Currently Amended) An apparatus comprising circuitry for use as a floating point adder configured to compute a result of a floating-point operation, wherein the apparatus receives an aligned addend comprising a plurality of bits and a plurality of products, the apparatus comprising:

a first circuit configured as a compound incrementer coupled to receive at least some of the plurality of bits of the aligned addend and a control signal, and configured to produce an output dependent upon the received bits of the aligned addend and the control signal;

a second circuit configured as a compression counter coupled to receive at least some of the plurality of bits of the aligned addend and the products and configured to produce an output dependent upon the received bits of the aligned addend and the received products;

a third circuit configured as a compound adder coupled to receive the output of the compression counter of the second circuit and configured to produce an output dependent upon the output of the compression counter of the second circuit;

a fourth circuit configured as a carry network coupled to receive sign bits of the products and the output of the compression counter of the second circuit and configured to produce an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter of the second circuit;

a fifth circuit configured as a selector coupled to receive at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network of the fourth circuit, wherein the selector is configured to produce a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

a sixth circuit configured as a plurality of multiplexers (muxes) coupled to receive the output of the compound incrementer of the first circuit, the output of the compound adder of the third circuit, and the selection signal produced by the selector of the fifth circuit, and configured to produce the result by selecting between the received output of the compound incrementer of the first circuit and the received output of the compound adder of the third circuit dependent upon the selection signal produced by the selector of the fifth circuit.

2. (Currently Amended) The apparatus of Claim 1, wherein the first circuit configured as the compound incrementer further comprises:

an incrementer coupled to receive at least some of the plurality of bits of the aligned addend and configured to produce an output dependent upon the received bits of the aligned addend and the control signal; and

a plurality of negation devices.

3. (Previously Presented) The apparatus of Claim 2, wherein one of the negation devices is coupled to receive the output of the incrementer and the control signal, and is configured to produce an output dependent upon the received output of the incrementer and the control signal.

4. (Previously Presented) The apparatus of Claim 2, wherein the plurality of negation devices implement exclusive-OR (XOR) logic functions.

5. (Original) The apparatus of Claim 2, wherein the plurality of negation devices are XOR-gates.

6. (Currently Amended) The apparatus of Claim 1, wherein the fourth circuit configured as the carry network further comprises:

logic coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter of the second circuit and configured to produce the carry signal dependent upon the received output of the compression counter of the second circuit.

7. (Currently Amended) The apparatus of Claim 1, wherein the fourth circuit configured as the carry network further comprises:

an XOR-gate coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter of the second circuit and configured to produce the carry signal dependent upon the received output of the compression counter of the second circuit.

8. (Currently Amended) The apparatus of Claim 1, wherein the fifth circuit configured as the selector is configured to produce a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

9. (Canceled).

10. (Currently Amended) The apparatus of Claim 1, wherein the output of the compound adder of the third circuit comprises a sum signal and an incremented sum signal, and one of the plurality of muxes of the sixth circuit is coupled to receive the sum signal from the compound adder of the third circuit, the incremented sum signal from the compound adder of the third circuit, and an inverted version of the sum signal , and is configured to produce at least a portion of the result.

11. (Canceled).

12. (Canceled).

13. (Original) The apparatus of Claim 1, wherein the compression device further comprises a 3:2 Counter.

14. (Currently Amended) The apparatus of Claim 4, wherein the second circuit configured as the compression counter compression device further comprises a 3:2 Counter.

15. (Canceled).

16. (Currently Amended) A computer program product, embodied on a computer readable medium, configured for use as a floating point adder for computing a result of a floating-point operation, wherein the computer program product receives an aligned addend comprising a plurality of bits and a plurality of products, the computer program comprising:

computer readable program code means for operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend and a control signal, and produces an output dependent upon the received bits of the aligned addend and the control signal;

computer readable program code means for operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products and produces an output

dependent upon the received bits of the aligned addend and the received products;

computer readable program code means for operating as a compound adder that receives the output of the compression counter and produces an output dependent upon the output of the compression counter;

computer readable program code means for operating as a carry network, wherein the carry network receives sign bits of the products and the output of the compression counter and produces an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

computer readable program code means for operating as a selector, wherein the selector receives at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, and wherein the selector produces a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

17. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as compound incrementer further comprises:

computer readable program code means for operating as an incrementer, wherein the incrementer receives at least some of the plurality of bits of the aligned addend and produce an output dependent upon the received bits of the aligned addend and the control signal; and

computer readable program code means for operating as a plurality of negation devices.

18. (Previously Presented) The computer program product of Claim 17, wherein one of the negation devices receives the output of the incrementer and the control signal, and produces an output dependent upon the received output of the incrementer and the control signal.

19. (Previously Presented) The computer program product of Claim 17, wherein the computer readable program code means for operating as the plurality of negation devices comprises computer readable program code means for implementing exclusive-OR (XOR) logic functions.

20. (Canceled).

21. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as the carry network further comprises:

computer readable program code means for operating as logic receiving the sign bits of the products and producing the output signal dependent upon the received sign bits of the products; and

computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

22. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as carry network further comprises:

computer readable program code means for operating as an XOR-gate, wherein the XOR-gate receives the sign bits of the products and produces the output signal dependent upon the received sign bits of the products; and

a computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

23. (Previously Presented) The computer program product of Claim 16, wherein the selector produces a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

24. (Canceled).

25. (Previously Presented) The computer program product of Claim 16, wherein the output of the compound adder comprises a sum signal and an incremented sum signal, and one of the plurality of muxes is coupled to receive the sum signal from the compound adder, the incremented sum signal from the compound adder, and an inverted version of the sum signal, and is configured to produce at least a portion of the result.

26. (Canceled).

27. (Canceled).

28. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as compression device further comprises computer readable program code means for operating as 3:2 Counter.

29. (Previously Presented) The computer program product of Claim 19, wherein the computer readable program code means for operating as compression device further comprises computer readable program code means for operating as 3:2 Counter.

30. (Canceled).